W600 Hardware Design Guide
V1.0.0

Beijing Winner Microelectronics Co., Ltd. (Winner Micro)

Addr: 18th Floor, Yindu Building, 67th Fucheng Road, Haidian District, Beijing, P.R.Chian

Tel: +86-10-62161900

Company Website: www.winnermicro.com

Document History

Version	Completion Date	Revision Record	Author	Auditor	Approver
V1.0.0	2018-10-25	Initial release	Linda	Ray	WM

Content

1 Overview

W600 integrates ARM CPU, rich peripheral interfaces, Wi-Fi MAC, Baseband, Security, RF. The chipset has rich functions and can meet the hardware requirement for IoT products. W600 is QFN32 package with the size 5mm x 5mm. Very few circuit devices are needed for the peripheral of the chip and a module can be designed with very small size.This design guide has introduced pin definition, physical size, timer, power, RF circuit and antenna etc. When customers begin to design products with W600, please strictly follow this guide, so as to get the best RF performance.

2 Pin Description

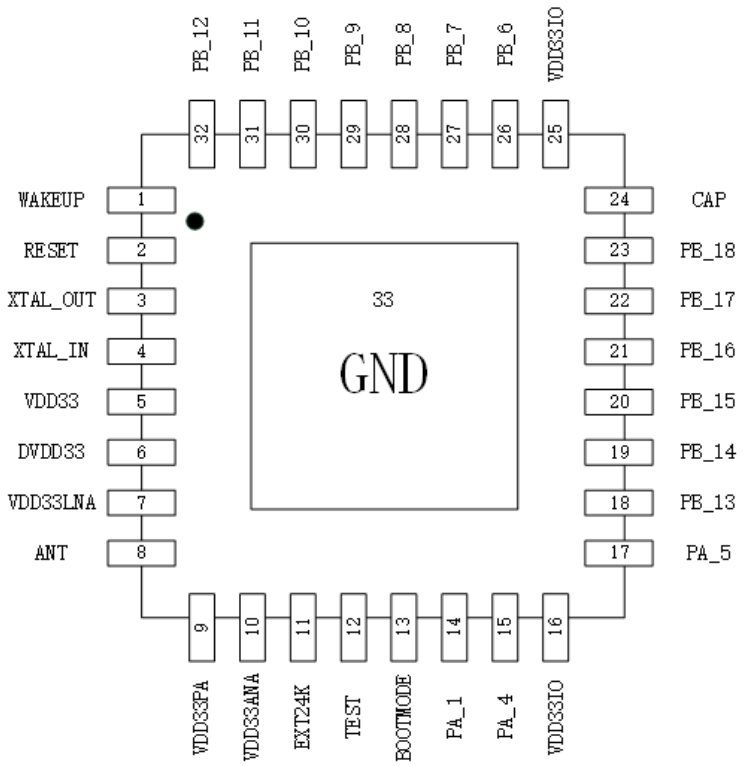

Figure 2-1 QFN32 Pin Diagram

Table 2-1 Pin Description

Pin No.	Pin Name	Type	Function Description after reset	Multi-function
1	WAKEUP	I	WAKEUP(wake up chipset by high level power)	
2	RESET	I	RESET(reset chipset by low level power)	
3	XTAL-OUT	O	Output External crystal oscillator	
4	XTAL-IN	I	input External crystal oscillator	
5	VDD33	P	power supply, 3.3V	
6	DVDD33	P	power supply for digital circuit, 3.3V	
7	VDD33LNA	P	power supply for LNA, 3.3V	
8	ANT	I/P	RF antenna	
9	VDD33PA	P	PA power supply, 3.3V	
10	VDD33ANA	P	power supply for analog circuit, 3.3V	
11	EXT24K	P	series connect with a resistor (24KΩ+-1%)	
12	TEST	I	Test mode	
13	PA_0	I/O	BOOTMODE	UART2_RX、PWM_1、GPIOPA_0
14	PA1	I/O	Reserved	SIM_DATA、PWM_2、SPI(M/S)_CK、GPIOPA_1
15	PA4	I/O	UART0_TX	PWM_5、SPI(M/S)_DO、I²S_M_SCL、GPIOPA_4
16	VDD33IO2	P	IO power supply,3.3V	
17	PA_5	I/O	UART0_RX	PWM_1、SPI(M/S)_DI、I²S_M_EXTCLK、GPIOPA_5
18	PB_13	I/O	PWM_2	I²C_SCL、SDIO_CMD、GPIOPB_13
19	PB_14	I/O	H_SPI_INT	PWM_5 、 I²C_DAT 、 I²S_S_SDA 、

				GPIOPB_14
20	PB_15	I/O	H_SPI_CS	PWM_4、SPI(M/S)_CS、I²S_S_SCL、GPIOPB_15
21	PB_16	I/O	H_SPI_CK	PWM_3、SPI(M/S)_CK、I²S_S_RL、GPIOPB_16
22	PB_17	I/O	H_SPI_DI	PWM_2、SPI(M/S)_DI、UART1_RX、GPIOPB_17
23	PB_18	I/O	H_SPI_DO	PWM_1、SPI(M/S)_DO、UART1_TX、GPIOPB_18
24	CAP	I	Capacitance,1μF	
25	VDD33IO1	P	IO power supply, 3.3V	
26	PB_6	I/O	Reserved	SWDAT、UART0_RX、PWM_4、SIM_CLK、GPIOPB_6
27	PB_7	I/O	Reserved	SWCK、UART0_TX、SDIO_CMD、SPI(M/S)_CS、GPIOPB_7
28	PB_8	I/O	PWM_5	H_SPI_CK、SDIO_CK、I²S_M_SCL、GPIOPB_8
29	PB_9	I/O	UART1_CTS	H_SPI_INT、SDIO_DAT0、I²S_M_SDA、GPIOPB_9
30	PB_10	I/O	UART1_RTS	H_SPI_CS、SDIO_DAT1、I²S_M_RL、GPIOPB_10
31	PB_11	I/O	UART1_RX	H_SPI_DI、SDIO_DAT2、I²C_SCL、GPIOPB_11
32	PB_12	I/O	UART1_TX	H_SPI_DO、SDIO_DAT3、I²C_DAT、GPIOPB_12
33	PAD	GND	Ground	

3 Periphery Circuit Design of W600

3.1 RESET Circuit Design

Reset circuit is proposed to design with RC circuit. W600 resets automatically by low level power. If RESET pin controlled by external circuit, the chipset will reset when the level is below 2.0V. The low level needs to last more than 100μs. See Figure 3-1.

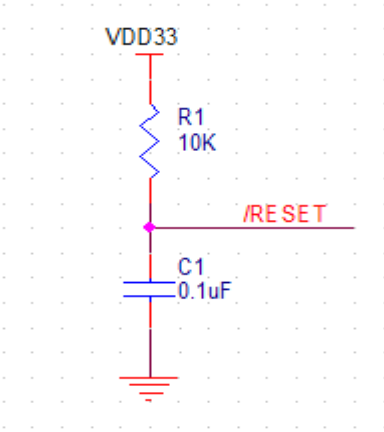

Figure 3-1 Reset circuit

3.2 Reference Clock Circuit Design

40MHz frequency is used for W600's reference clock which should be -40~85℃/±10ppm with 10pF load capacitance. See figure 3-2。

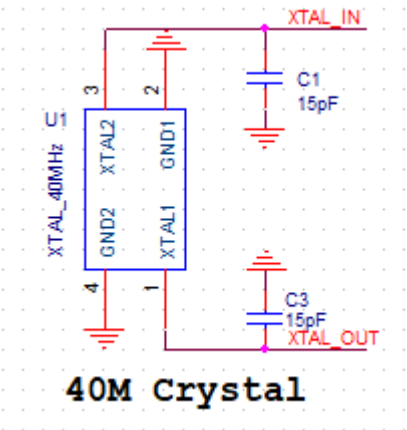

Figure 3-2 Crystal oscillator circuit

Clock routing is as close to the chip as possible, as short as possible, and leave away from interference source. All other routes are prohibited to be layed below the clock to prevent interference with clock source.

3.3 RF Circuit Design

The chipset is designed with a single antenna. W600 integrates PA and transceiver switch.

The impedance of the antenna port is 50Ω. According to the performance requirement of module design, it is suggested to use π type design to match the circuit. External elements should be optimized according to the actual antenna impedance value.

In order to save cost, customers can use two-layer board design with FR-4 board and 0.8mm thickness. In order to achieve 50Ω of RF wiring impedance, the wire width should be 20mil, the distance from wire to copper should be 5mil. RF routing is on top layer. No other routing can be used on the back of RF routing, and copper should be covered the back of RF routing to ensure the integrity of RF reference GND.

3.4 GPIO Design

After the chiset is power on, the pin15 and pin17 is default for UART0 port. Firmware downloading, AT+command and output debugging log can be used with this port. Customers should be careful not to use this port as GPIO if you want to use this port to download or debug. Ater the whole system is in operation, this port can be reused for other ports.

Table 3-2 UART0 Port Description

15	PA4	I/O	UART0_TX
17	PA_5	I/O	UART0_RX

Other reused pins can refer to Table 2-1.

3.5 Power Circuit Design

The input foot of the chip's power supply is equipped with the corresponding filter capacitor, and the total current of whole chip power supply is recommended to be 500mA or more. The wiring width shoude not be less than 30mil. The power supply range is 3.0V~3.6V. Over 3.6V may cause permanent damage to the chip. Lower than 3.0V may cause whole performance degradation. The reference design can see the following tables.

A 10μf and a 4.7nf fitler capacitors should be placed near pin5, pin6, pin7. See table 3-3.

Table 3-3 Power Pin Description

5	VDD33	P	POWER, 3.3V	
6	DVDD33	P	Digital circuit power, 3.3V	
7	VDD33LNA	P	LNA power, 3.3V	

A 47μf filter capacitor should be placed near pin9 and pin10. We suggest customer to place a

330μf electrolytic capacitor on their base board. See table 3-4.

Table 3-4 Power PIN Description

9	VDD33PA	P	PA power, 3.3V	
10	VDD33ANA	P	Analog power, 3.3V	

Pin24 need an external 1μf filter capacitor.

Pin11 need an external 24K resistance with the accuracy 1%.

3.6 GND Design

The PAD in the middle of W600 is for heat sinking and has to connect with GND and need to add drilling. See figure 3-3 and figure 3-4

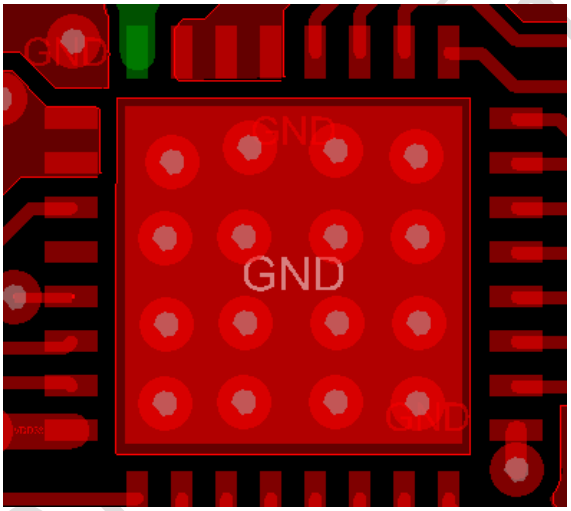

Figure 3-3 GND design

After the product design is completed, it needs all layers PCB to be copper-coated grounding treatment, and let as few as possible routing go though the back of the chip.

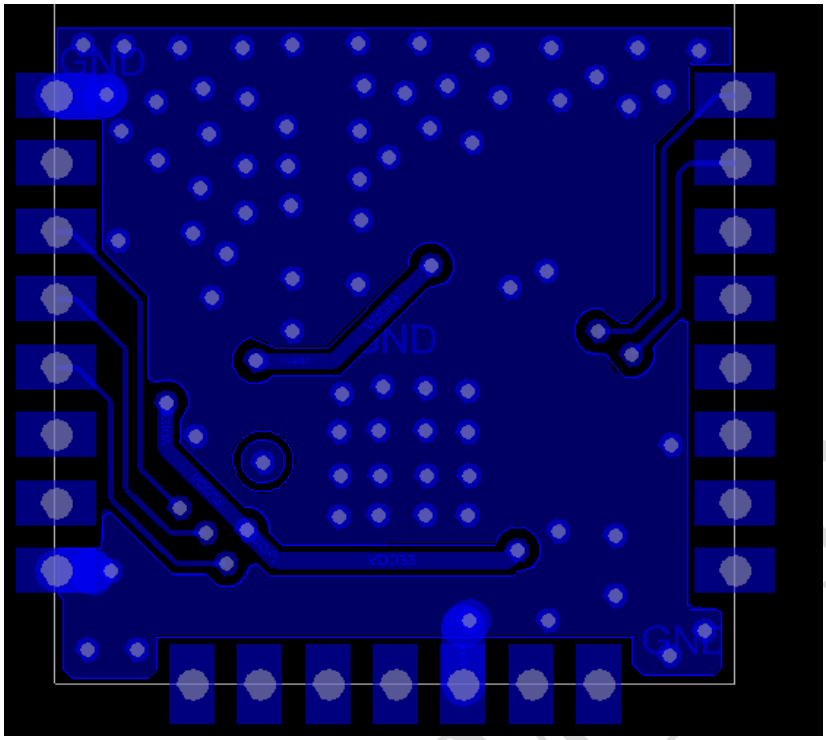

Figure 3-4 GND design

3.7 Antenna Design

Both external antenna and PCB antenna can be used for module design.

3.7.1 External antenna

The connecting seat of the external antenna is as far away as possible from the noise sources such as the power interfenrence from bottom board power and other noice souces.

3.7.2 PCB antenna

The design of PCB antenna should be strictly in accordance with this user guide to prevent antenna performance degradation. Copper coating on the back of the antenna should be hollowed out. The antenna reference ground should be as large as possible. The PCB antenna should be simulated in practice. The antenna size map should be imported into module PCB after simulation. All layers of antenna area can not be covered with copper. See figure 3-5.

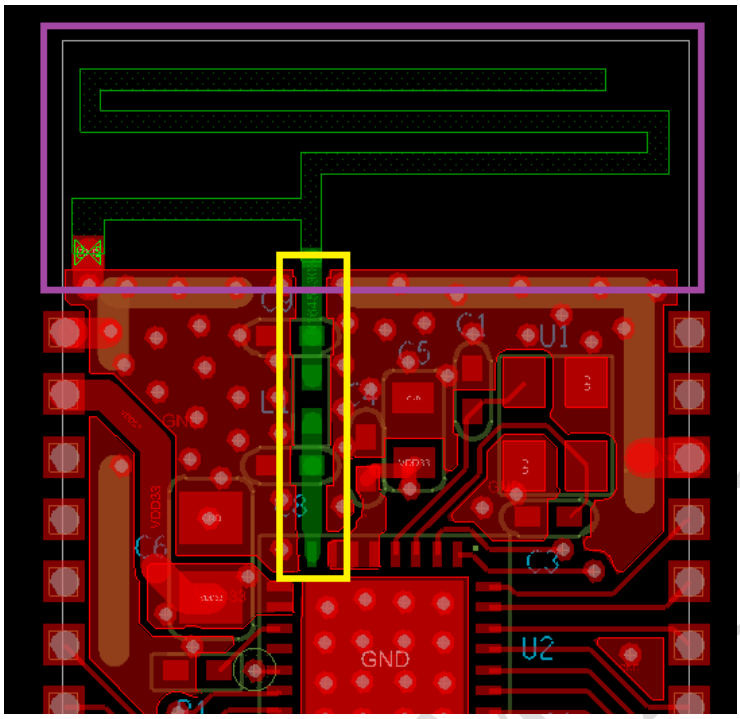

Figure 3-5 PCB antenna design

Figure 3-6 and 3-7 are 2 antenna placement modes which can add very little effect on performance of antenna. We suggest customers to choose one of these 2 modes to design the placement. For the second placement mode, PCB antenna should be at least 5.0mm from both sides of the bottom board.

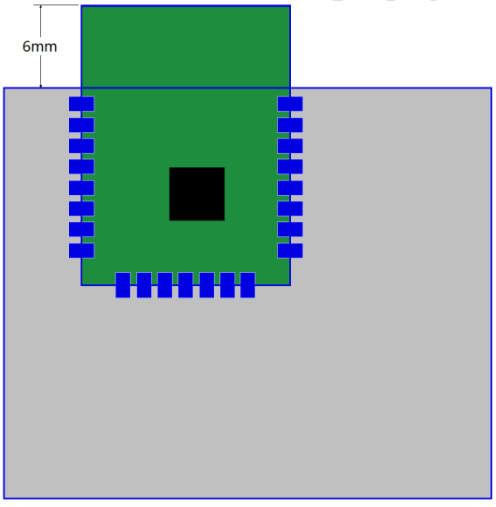

Figure 3-6

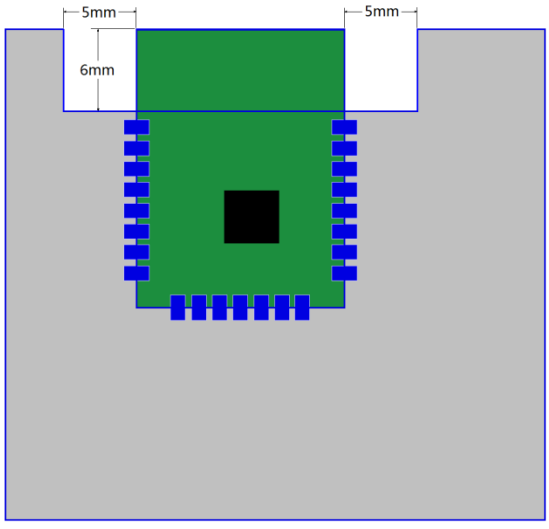

Figure 3-7